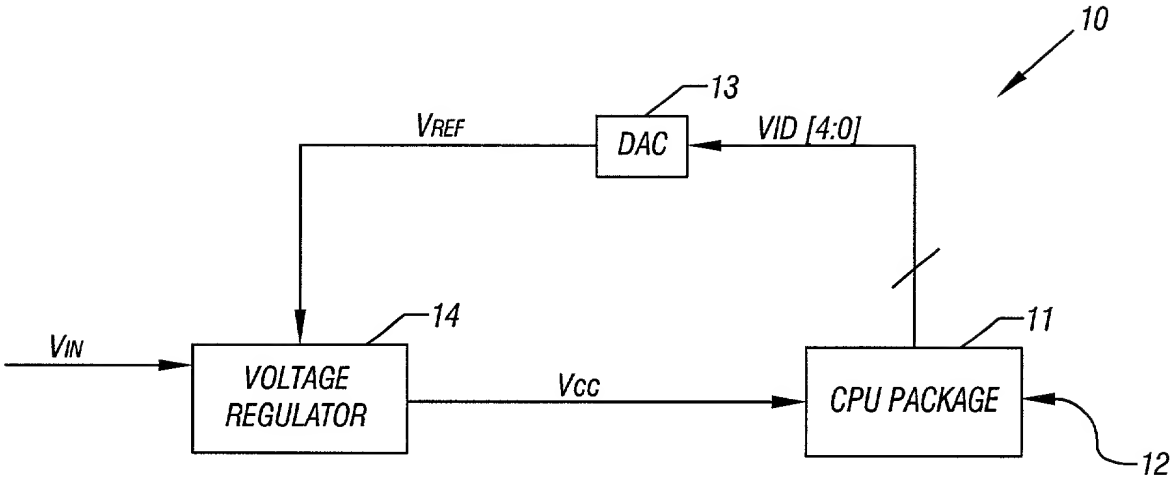

FIG. 1
(PRIOR ART)

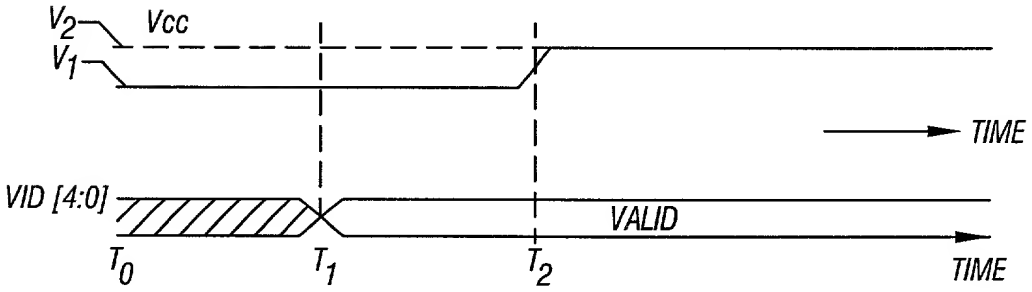

FIG. 4

FIG. 5

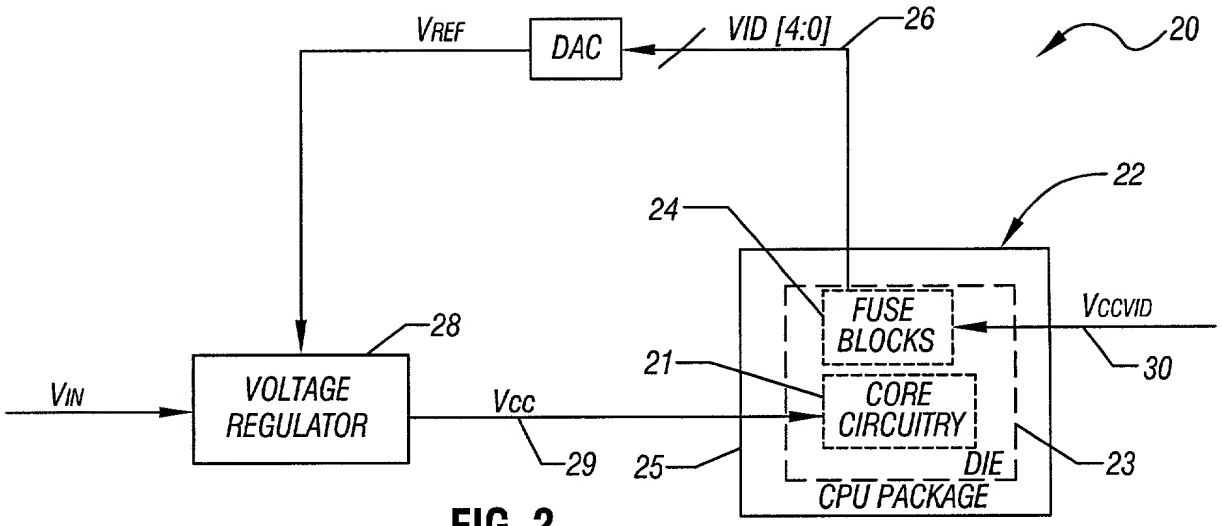
VREF
DAC
VID [4:0]
26
20
22
24
FUSE BLOCKS
VCCVID
30
28
21
VOLTAGE REGULATOR
VIN
VCC
CORE CIRCUITRY
29
25
DIE
23
CPU PACKAGE

FIG. 2

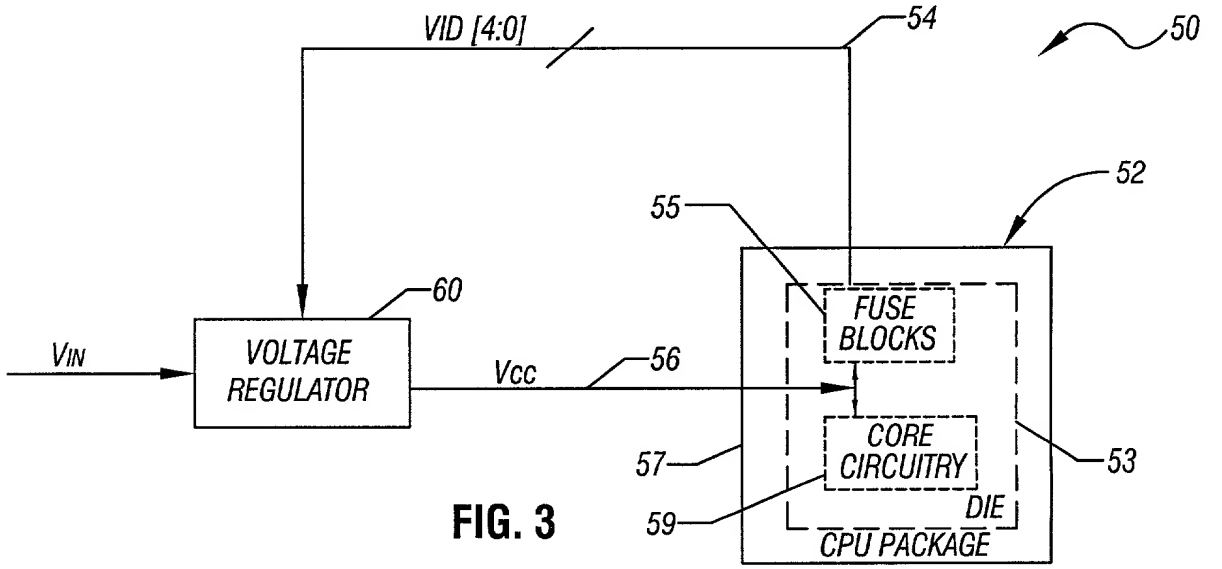
VID [4:0]
54
50
52
55
FUSE BLOCKS
60
VOLTAGE REGULATOR
VIN
VCC
56
CORE CIRCUITRY
57
53
59
DIE
CPU PACKAGE

FIG. 3

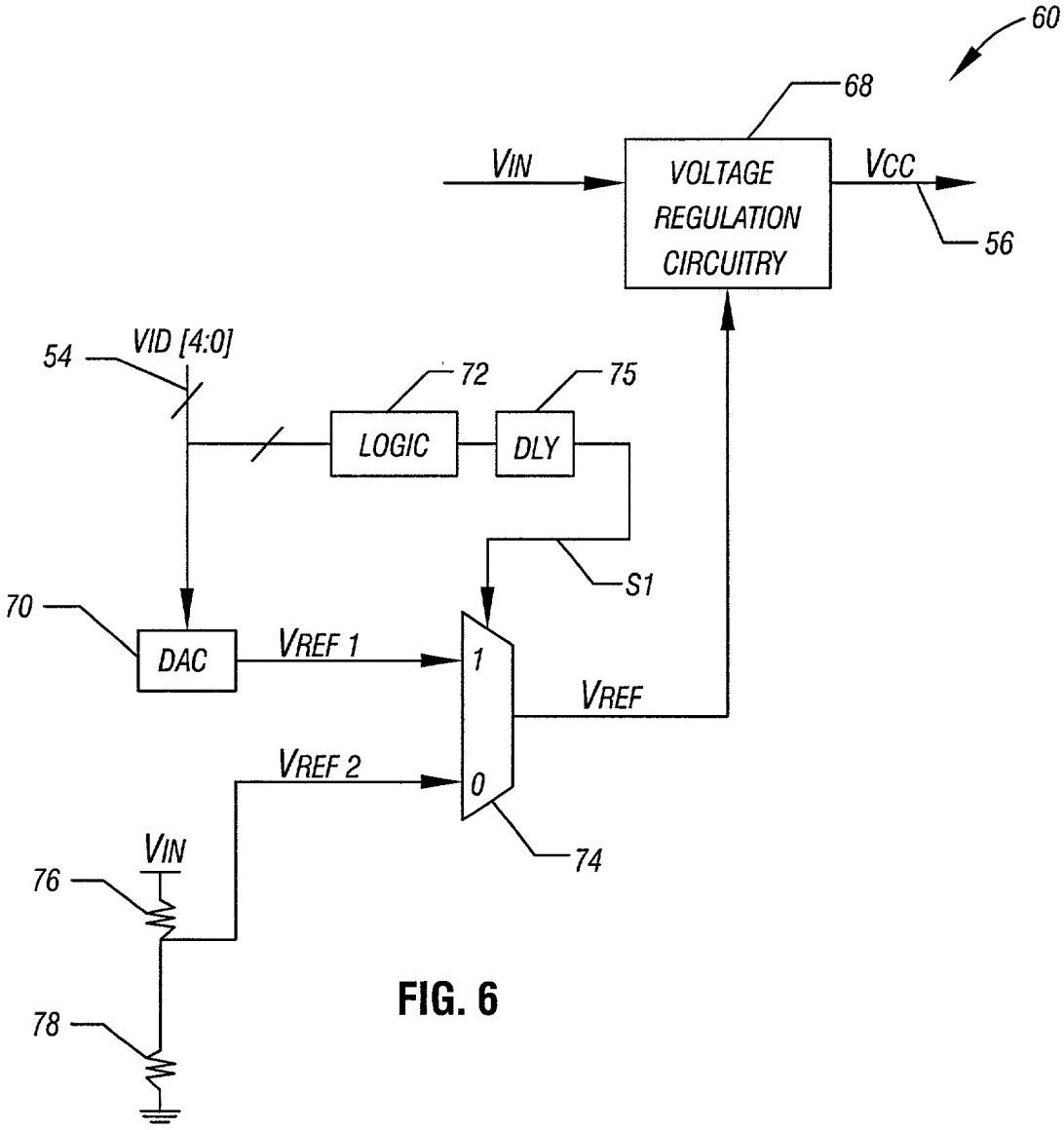
60
68
VIN
VOLTAGE REGULATION CIRCUITRY
VCC
56
54
VID [4:0]
72
LOGIC
75
DLY
S1
70
DAC
VREF 1
1
VREF
VREF 2
0
74
VIN
76
78

FIG. 6

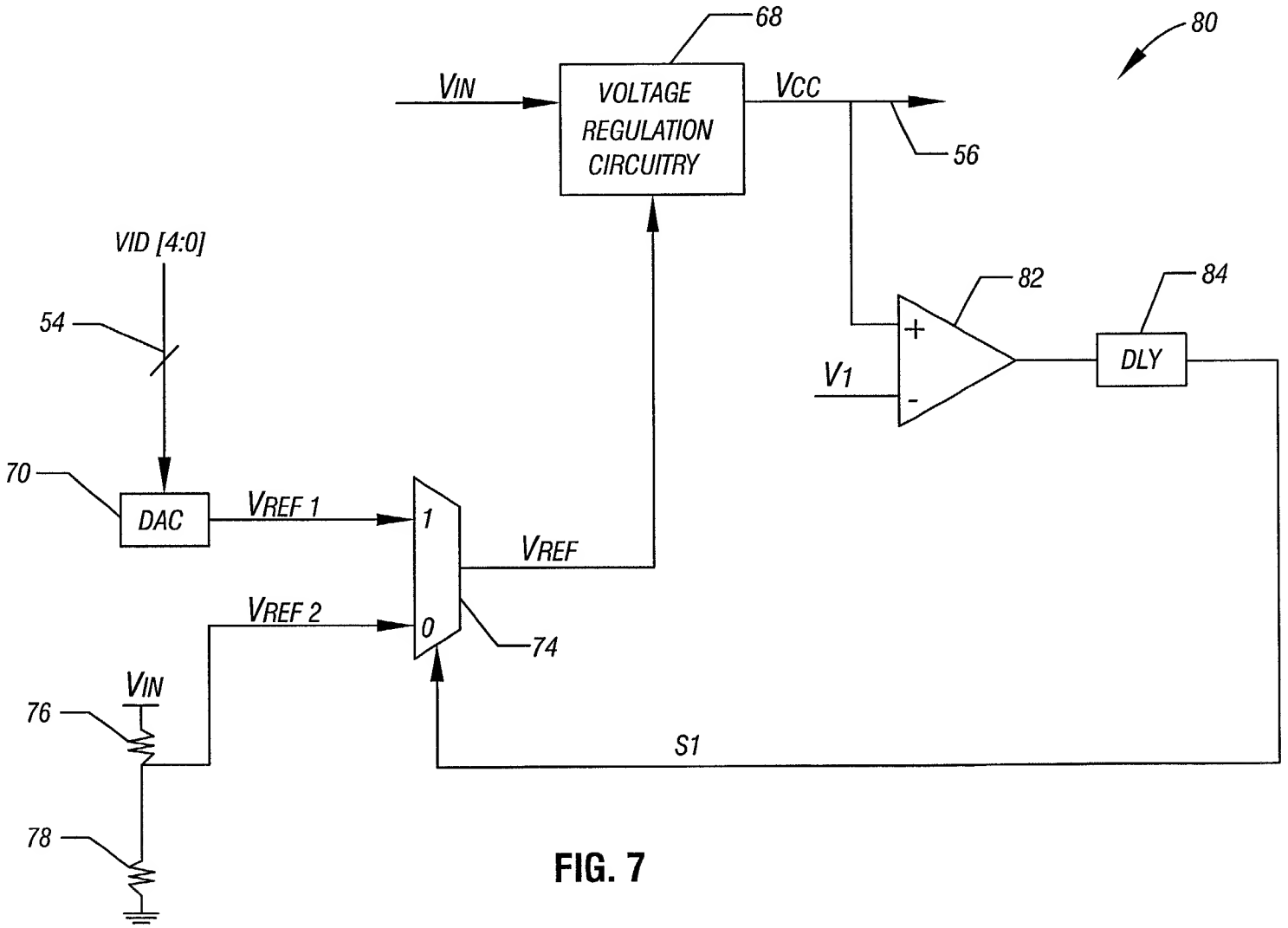

FIG. 7

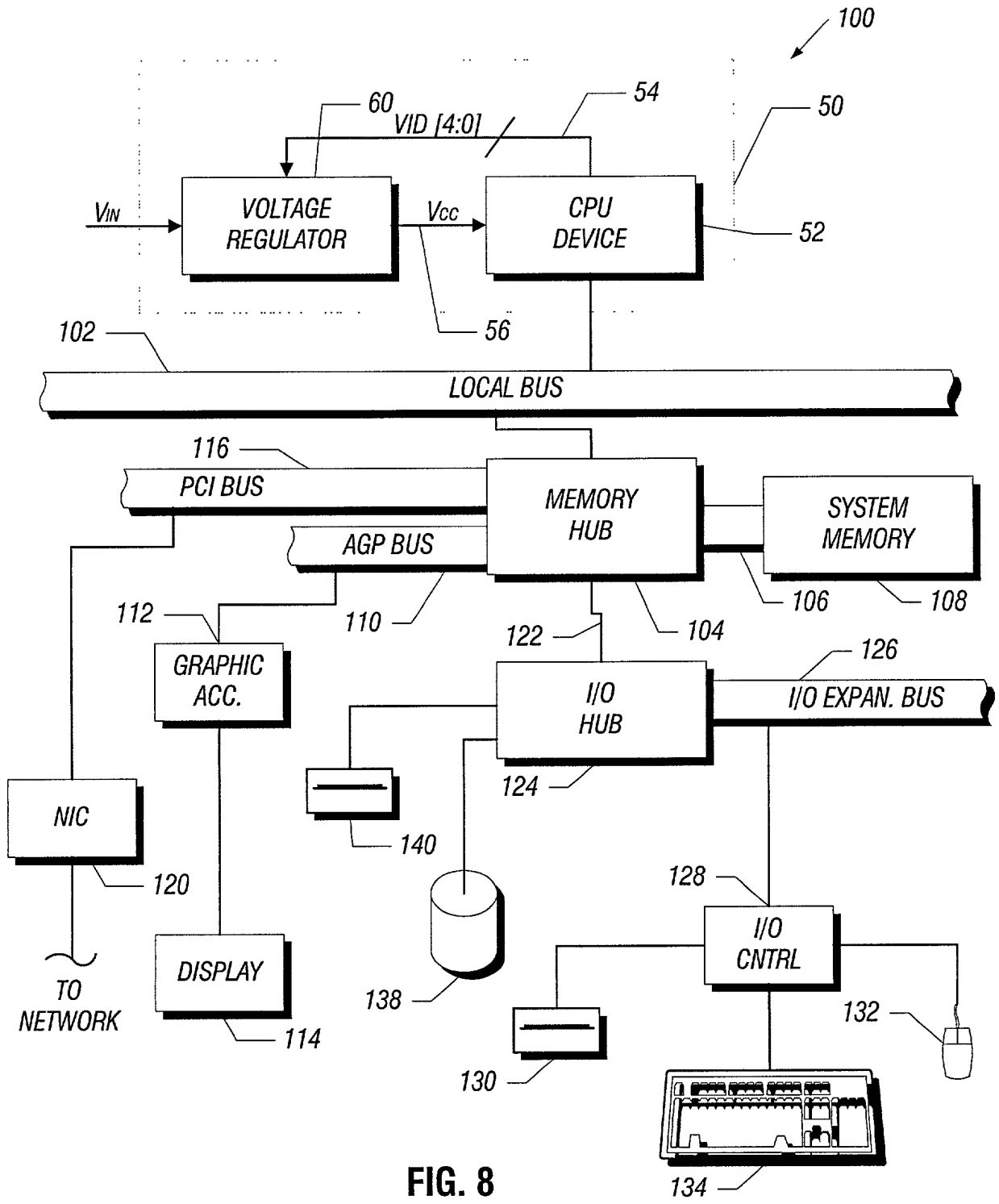
100
60
VID [4:0]
54
50
VIN
VOLTAGE REGULATOR
VCC
CPU DEVICE
52
56
102
LOCAL BUS
116
PCI BUS
AGP BUS
MEMORY HUB
SYSTEM MEMORY
106
108
112
110
122
104
126
GRAPHIC ACC.
I/O HUB
I/O EXPAN. BUS
124
NIC
140
120
128
I/O CNTRL
TO NETWORK
DISPLAY
138
132
130
114
134

FIG. 8